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98

SEARCH REQUEST FORM Scientific and Technical Information Center

Requester's Full Name: Eric B. Kiss Examiner#: 796 11 Date: 8/23/2002
 Art Unit: 2122 Phone Number: 305-7737 Serial Number: 09/521,280
 Mail Box and Bldg/Room Location: PK2 5B46 Results Format Preferred (circle): Paper Disk E-mail

If more than one search is submitted, please prioritize searches in order of need.

Please provide a detailed statement of the search topic, and describe as specifically as possible the subject matter to be searched. Include the elected species or structures, keywords, synonyms, acronyms, and registry numbers, and combine with the concept or utility of the invention. Define any terms that may have a special meaning. Give examples or relevant citations, authors, etc., if known. Please attach a copy of the cover sheet, pertinent claims, and abstract.

Title of Invention: TCL-PLI, A Framework for Reusable, Run Time Configurable Test Benches
 Inventors (please provide full names): Stephan Voges and Mark Andrews

Earliest Priority Filing Date: 3/7/2000

**For Sequence Searches Only* Please include all pertinent information (parent, child, divisional, or issued patent numbers) along with the appropriate serial number.*

- Use of TCL Scripting language with Verilog (a hardware descriptive language (HDL)) for the purpose of run-time configuring
- Found NC-Verilog product by Cadence, but unable to locate documentation and technical details.

08-23-02 P01:19 IN

• Attached: Abstract and claims 1-30

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Online Time: <u>4 hours</u>	Other _____	Other (specify) <u>STIC Catalog</u>

September 5, 2002

Dear Mr. Kiss,

Attached please find the results of your search request for application #09/521,280. I concentrated on finding user manual's for the various test bench environments you indicated along with others that might be available. I searched the Internet along with the STIC online catalog.

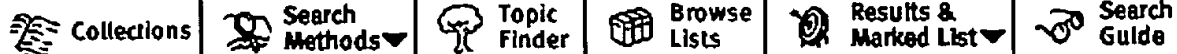
Please let me know if you have any questions.

Regards,

A handwritten signature in cursive script that reads "Geoffrey St. Leger".

Geoffrey St. Leger
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

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- ☐ 3.    [Place-and-route tool targets very-deep-submicron database](#); *Cheryl Ajluni*; **Electronic Design**, Cleveland; Mar 9, 1998; Vol. 46, Iss. 6; pg. 91, 2 pgs
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- ☐ 5.   [Chrysalis Delivers New Model Checking Tool for On-Chip Interfaces and Protocols](#); *Business/Technology Editors*; **Business Wire**, New York; Feb 23, 1998; pg. 1
- ☐ 6.    [Design software](#); *Judy Erkanat*; **Electronic News**, New York; Jul 21, 1997; Vol. 43, Iss. 2177; pg. 35, 1 pgs
- ☐ 7.    [Project automation/management tools make designers' jobs easier](#); *Cheryl Ajluni*; **Electronic Design**, Cleveland; Jul 7, 1997; Vol. 45, Iss. 14; pg. 49, 7 pgs
- ☐ 8.    [Design software](#); *Judy Erkanat*; **Electronic News**, New York; Apr 21, 1997; Vol. 43, Iss. 2164; pg. 28, 1 pgs
- ☐ 9.   [HDL automation targets network designs](#); *Steve Carlson, Director of High-Level Design Methodology, Dirk Seynhaeve, Director of Corporate Applications and Lalgudi Kannan, Principal Engineer, Escalade Corp., Santa Clara, Calif.*; **Electronic Engineering Times**, Manhasset; Nov 11, 1996; pg. 48
- ☐ 10.    [HDL automation targets network designs](#); *Carlson, Steve*; **Electronic Engineering Times**, Manhasset; Nov 11, 1996, Iss. 927; pg. 48, 1 pgs

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VLSI Test Symposium, 2002. (VTS 2002). Proceedings 20th IEEE , 2002

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[\[Abstract\]](#) [\[PDF Full-Text \(375 KB\)\]](#) **CNF****2 An evolutionary algorithm for the multi-objective optimisation of VLSI primitive operator filters***Thomson, R.; Arslan, T.*

Evolutionary Computation, 2002. CEC '02. Proceedings of the 2002 Congress on , Volume: 1 , 2002

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[\[Abstract\]](#) [\[PDF Full-Text \(645 KB\)\]](#) **CNF****3 Language design requirements for VHDL-RF/MW/sup TM/***Willis, J.; Johnson, J.*

Microwave Symposium Digest, 2002 IEEE MTT-S International , Volume: 3 , 2002

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[\[Abstract\]](#) [\[PDF Full-Text \(365 KB\)\]](#) **CNF****4 A methodology for automated insertion of concurrent error detection hardware in synthesizable verilog RTL***Mohanram, K.; Krishna, C.V.; Toubia, N.A.*

Circuits and Systems, 2002. ISCAS 2002. IEEE International Symposium on , Volume: 1 , 2002

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1 Integrating Perl, Tcl and C++ into simulation-based ASIC verification environments

McKinney, M.D.

High-Level Design Validation and Test Workshop, 2001. Proceedings. Sixth IEEE International , 2001

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